Rijoy Mukherjee

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Education

July 2019 – present	**PhD: Indian Institute of Technology Kharagpur**
	Computer Science and Engineering.
	CGPA : 8.96
	Advisor: Dr. Rajat Subhra Chakraborty
July 2012 – May 2016	**B.Tech: National Institute of Technology Durgapur**
	Computer Science and Engineering.
	CGPA : 8.84
	Advisor: Dr. Bibhash Sen
	Thesis title: *On the Reliability of Majority Logic Structure in Quantum-dot Cellular Automata*
2012	**Senior Secondary: Hem Sheela Model School Durgapur**
	Board : *CBSE*
	Percentage: 93.4
2010	**Secondary: St. Peter's School Durgapur**
	Board : *ICSE*
	Percentage: 85.86

Research Publications

Journal Articles

1. **Mukherjee**, **R.**, & Chakraborty, R. S. (2022). Novel Hardware Trojan Attack on Activation Parameters of FPGA-based DNN Accelerators. *IEEE Embedded Systems Letters*, 1–1.
   🔗 https://doi.org/10.1109/LES.2022.3159541

2. **Mukherjee**, **R.**, Govindan, V., Koteshwara, S., Das, A., Parhi, K. K., & Chakraborty, R. S. (2020). **Probabilistic Hardware Trojan Attacks on Multiple Layers of Reconfigurable Network Infrastructure**. *Journal of Hardware and Systems Security*, 4(4), 343–360.
   🔗 https://doi.org/10.1007/s41635-020-00107-9

3. Sen, B., Chowdhury, M. R., **Mukherjee**, **R.**, Goswami, M., & Sikdar, B. K. (2017). **Reliability-aware design for programmable QCA logic with scalable clocking circuit**. *Journal of Computational Electronics*, 16(2), 473–485. 🔗 https://doi.org/10.1007/s10825-017-0973-z

4. Goswami, M., Sen, B., **Mukherjee**, **R.**, & Sikdar, B. K. (2017). **Design of Testable Adder in Quantum-dot Cellular Automata with Fault Secure Logic**. *Microelectronics Journal*, 60, 1–12.
   🔗 https://doi.org/https://doi.org/10.1016/j.mejo.2016.11.008

5. Sen, B., **Mukherjee**, **R.**, Mohit, K., & Sikdar, B. K. (2017). **Design of reliable universal QCA logic in the presence of cell deposition defect**. *International Journal of Electronics*, 104(8), https://doi.org/10.1080/00207217.2017.1293174, 1285–1297.
   🔗 https://doi.org/10.1080/00207217.2017.1293174

6. Sen, B., Dutta, M., **Mukherjee**, **R.**, Nath, R. K., Sinha, A. P., & Sikdar, B. K. (2016). **Towards the design of hybrid QCA tiles targeting high fault tolerance**. *Journal of Computational Electronics*, 15(2), 429–445. 🔗 https://doi.org/10.1007/s10825-015-0760-7

7   Sen, B., Sahu, Y., **Mukherjee**, **R.**, Nath, R. K., & Sikdar, B. K. (2016). **On the reliability of majority logic structure in quantum-dot cellular automata**. *Microelectronics Journal*, *47*, 7–18. 🔗 https://doi.org/https://doi.org/10.1016/j.mejo.2015.11.002

Conference Proceedings

1   Santikellur, P., **Mukherjee**, **R.**, & Chakraborty, R. S. (2021). Apuf-bnn: An automated framework for efficient combinational logic based implementation of arbiter puf through binarized neural network, In *Proceedings of the 2021 on great lakes symposium on vlsi*, New York, NY, USA, Association for Computing Machinery. 🔗 https://doi.org/10.1145/3453688.3461484

2   Rajendran, S. R., **Mukherjee**, **R.**, & Chakraborty, R. S. (2020). **SoK: Physical and Logic Testing Techniques for Hardware Trojan Detection**, In *Proceedings of the 4th acm workshop on attacks and solutions in hardware security*, Virtual Event, USA, Association for Computing Machinery. 🔗 https://doi.org/10.1145/3411504.3421211

3   **Mukherjee**, **R.**, Tripathi, S., Sen, S., & Sen, B. (2016). **Characterization and analysis of single electron fault of QCA primitives**, In *2016 international conference on microelectronics, computing and communications (microcom)*.

4   Sen, B., Nath, R. K., **Mukherjee**, **R.**, Sahu, Y., & Sikdar, B. K. (2016). **Towards Designing Reliable Universal QCA Logic in the Presence of Cell Deposition Defect**, In *2016 29th international conference on vlsi design and 2016 15th international conference on embedded systems (vlsid)*.

5   Sen, B., Agarwal, A., Nath, R. K., **Mukherjee**, **R.**, & Sikdar, B. K. (2014). **Efficient design of fault tolerant tiles in QCA**, In *2014 annual ieee india conference (indicon)*.

6   Sen, B., **Mukherjee**, **R.**, Nath, R. K., & Sikdar, B. K. (2014). **Design of Fault Tolerant Universal Logic in QCA**, In *2014 fifth international symposium on electronic system design*.

Skills

Coding	▮	C, C++, Java, Python
Misc.	▮	LaTeX, GnuPlot, Vector drawing

Achievements

2019	▮	**GATE,** All India Rank : 308, Score : 777
2012	▮	**AIEEE,** All India Rank : 15452, State Rank : 413
	▮	**WBJEE,** Rank : 1500

Professional Experience

July. 2016 – July. 2019   ▮   **Software Engineer.** Dynamic Digital Technology, Kolkata, West Bengal

References

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Indian Institute of Technology Kharagpur.
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